CLAIMS

1. A decoder for a trellis code, comprising:

a path metrics calculation unit for calculating path metrics over at least two trellis columns in a trellis, the path metrics calculation unit including an input interface for old path metrics and an output interface for new path metrics;

a memory for storing path metrics of the trellis, the memory including a read interface for reading old path metrics from the memory and a write interface for writing new path metrics into the memory;

an input multiplexer connected between the read interface of the memory and the input interface of the path metrics calculation unit;

an output multiplexer connected between the output interface of the path metrics calculation unit and the write interface of the memory; and

a control for controlling configuration of the input multiplexer and configuration of the output multiplexer on the basis of states of the trellis, which state of the trellis defines the way the old path metrics and the new path metrics relate to each other, whereby internal configuration of the path metrics calculation unit remains the same for different code constraint lengths.

2. A decoder according to claim 1, wherein the control includes a binary counter representing a state of the trellis, and the control depends on the bit values of predetermined positions in the binary counter.

3. A decoder according to claim 1, wherein the multiplexer includes as many interconnected sub-multiplexers as there are trellis columns over which the path metrics are calculated.

4. A decoder according to claim 1, wherein the multiplexer includes two interconnected sub-multiplexers, wherein in the first sub-multiplexer two neighboring buses exchange data and in the second sub-multiplexer two neighboring bus pairs exchange data.

5. A decoder according to claim 4, wherein the multiplexer further includes a third sub-multiplexer that exchanges data between two groups, each having four adjoining buses.